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# 64-channel pre-amplifier ASICs for superconducting tunnel junction readout

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**Abstract**

Superconducting Tunnel Junctions (STJ) have been extensively investigated as photon detectors covering the range from near-infrared to X-ray energies. STJ detector developments now focus on the integration of many devices into large imaging arrays. However, current state-of-the-art preamplifier electronics for these detectors still rely on circuits build from discrete components. We are reporting here on a first attempt to integrate such circuits into an application-specific integrated circuit (ASIC). Two ASICs have been developed. One consists of 64 low-noise, low-offset pre-amplifier channels, while the other contains the same number of shaping filters and threshold detection circuits.


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## 1. Introduction

Superconducting Tunnel Junctions (STJs) have been shown to be efficient photon detectors from the near infrared to X-ray energies [1,2]. Photo-absorption in superconductors occurs in a similar manner to that in semiconductors in that excitations (quasiparticles) are generated in a number proportional to the absorbed photon energy. However, the energy required to generate quasi-particles in superconducting Tantalum is about three orders of magnitude lower than that needed to generate free carriers in, e.g., silicon detectors. The energy of incoming photons can thus be measured accurately by integrating the collected charge with a charge-sensitive amplifier.

The major complexity associated with reading out these devices is related to providing a low and stable bias voltage in the range of $\sim 100\,\mu V$ while minimizing noise sources. Traditionally, this is achieved by using amplifiers built from discrete components. The input stage consists of a silicon JFET for low-noise operation while a low-offset voltage, low-noise operational amplifier controls the detector's bias voltage in a DC feedback loop [1].

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Current developments on STJ detectors focus on the design of large imaging arrays. A 120 pixel device is being used already in an optical photo-spectrometer [3]. Clearly there is a need now to develop highly integrated readout electronics. For this purpose, two ASICs were designed under ESA contract at IDEAS, Norway [4].

## 2. The VA64SARA

The VA64SARA ASIC is a 64-channel low-noise, low-power charge-sensitive preamplifier circuit. This chip was specifically designed to readout STJs operating as photon detectors in the visible and UV wavelength range. Each amplifier channel further includes a low-pass (anti-aliasing) filter, output buffer, input bias voltage control and a leakage current compensation circuit. The ASIC occupies an area of $\sim 8.2 \times 7.3\,\mathrm{mm}^2$ and is implemented in a 0.8 μm N-well CMOS double poly, double metal AMS process [5].

In the micrograph shown in Fig. 1, analog input and output pads are on the left and right, respectively. Top and bottom pads are reserved for the digital signals and chip bias voltages.

The chip requires separate $\pm 2$ V supplies for the analog and digital parts. Total nominal power consumption is 400 mW or $\sim 6$ mW/channel.

Only about one-third of the chip's area (left in the picture) is needed for the actual amplifiers, whereas the rest of the chip consists of the digital-to-analog converters (DACs) used for controlling the input offset voltage and detector bias. These DACs, one for each channel, have 10 bits resolution. This allows for a nominal offset adjustment range of $\pm 5$ mV and a resolution of $\pm 5$ μV. The actual range and resolution is externally controllable by a bias current.

A calibration routine is executed after power-up, which measures the input offset values and corrects the DAC settings. Since changing a particular DAC value has a small influence on the others, due to different drawn current values, an iterative procedure is required. Typically, 5–6 iterations are required to reduce the offset voltages below 10 μV. Fig. 2 shows the results obtained after 15 iterations for each of the 64 channels on 2 separate chips.

The left axis is the residual offset voltage while the right axis shows the digital DAC values. Chip 2 can clearly be compensated correctly (only 1 bad channel) while many DAC values saturate (at 0) for chip 1, hence this ASIC is not usable. Offset voltages are very stable over time and are primarily dominated by temperature fluctuations. Less than $\pm 15$ μV drifts have been observed in the laboratory over a period of $> 15$ h, without taking

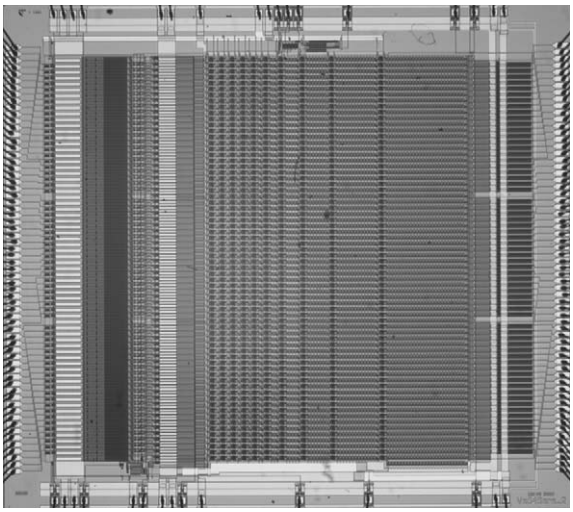

Fig. 1. VA64SARA micrograph.

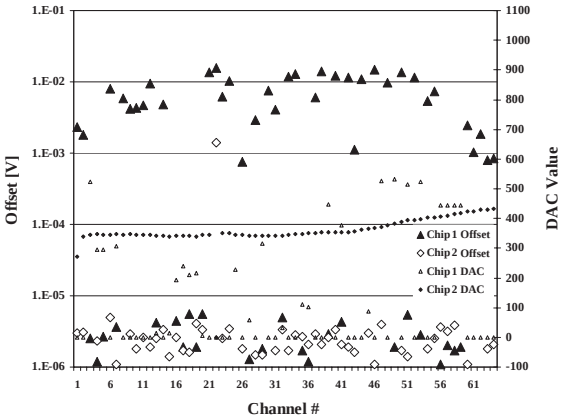


Fig. 2. Offset, in volts and corresponding digital DAC values for 2 chips. Offsets on chip 1 cannot be correctly compensated, whereas for chip 2, only 1 channel is out of specification.

special precautions for stabilizing the environment's temperature.

The equivalent input noise charge (ENC) measured with a 10 μs peaking time shaping filter is $250e^-_{rms}$ with a noise slope of $2.9e^-_{rms}/pF$. For a typical detector and wiring capacitance of 100 pF, the ENC is $540e^-_{rms}$. These low noise values are obtained by using a folded cascode input stage with a $W/L = 12000/1.4\,\mu m/\mu m$ PMOS input transistor. The bias current for this transistor is set to 2.2 mA which yields a simulated transconductance of ~30 mS. With a total current of 2.5 mA in the input cascode pair, most of the power is dissipated in these transistors.

The charge integrator contains a 200 fF feedback capacitance. Combined with an additional gain stage, the chip's gain is 13 mV/fC. Its dynamic range is ±100 fC.

## 3. The TA64SARA

In order to separate fast digital transients from the very sensitive front-end amplifiers, a separate chip was designed for detecting signals above threshold. The TA64SARA contains 64 parallel triggering circuits that can be directly matched to the VA64SARA. A single channel schematic of both ASICs is given in Fig. 3.

The TA64SARA includes for each channel, a CR-RC shaper followed by a level-sensitive discriminator and address encoder. Once a signal is detected above threshold, the chip generates a trigger and the channel's address is loaded onto the address bus. The trigger signals from all channels are wire-or'ed to a single trigger signal.

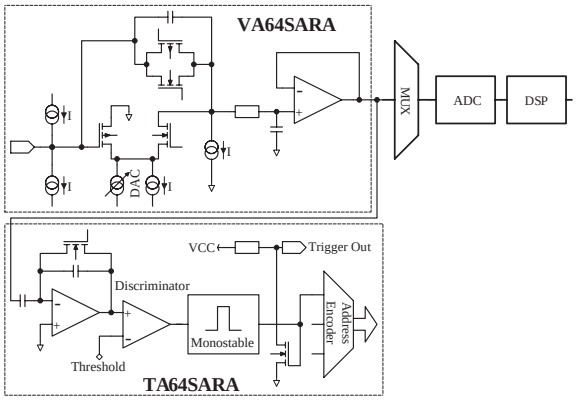


Fig. 3. Single-channel VA64SARA and TA64SARA schematic.

This circuit also requires separate ±2 V supplies for the analog and digital parts. Power consumption is ~1 mW/channel.

The chip has an area of $4.7 \times 5.2\,mm^2$ and is implemented in the same CMOS process as the VA64SARA.

The shaping amplifier has a tunable peaking time in the range 3–9 μs. This allows for matching the filter's bandwidth to the STJ signals.

In the particular application of optical photon detection with STJs, the recorded signals for the longest wavelengths are so low that the trigger level needs to be set to very low values, near the noise edge. In order to provide uniform and the lowest possible threshold setting, the offset of each discriminator can be compensated by a 3-bit DAC. The resolution of these DACs is tunable by an external current source. Furthermore, each channel can be enabled or disabled individually by a bit mask.

Digital settings are programmed into the chip using a shift register. The last element of this register is also available on an output pad. This allows us to control its status but also to daisy-chain a number of chips.

## 4. Conclusions

Two ASICs, each having 64 independent channels, have been designed. The first chip provides detector biasing and low-noise signal amplification while the threshold detection and trigger logic is implemented in the second one. Although a standard CMOS process was used, the design allows for input offset voltage compensation to within ±10 μV. The low noise operation ($\sim 500e^-_{rms}$), comparable to our state-of-the-art discrete amplifiers, permits optical photon detection from Superconducting Tunnel Junctions. In comparison to traditional discrete amplifiers, the compactness of the chips and their low power consumption are a major step forward to readout large format STJ arrays.

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